Nano
Wafer Level
Packaging

An International Research and Educational Collaboration between

National University of Singapore
Institute of Microelectronics, Singapore
Georgia Tech Packaging Research Center, U.S.A.

Sponsored as a Temasek Professorship by A* STAR, Singapore

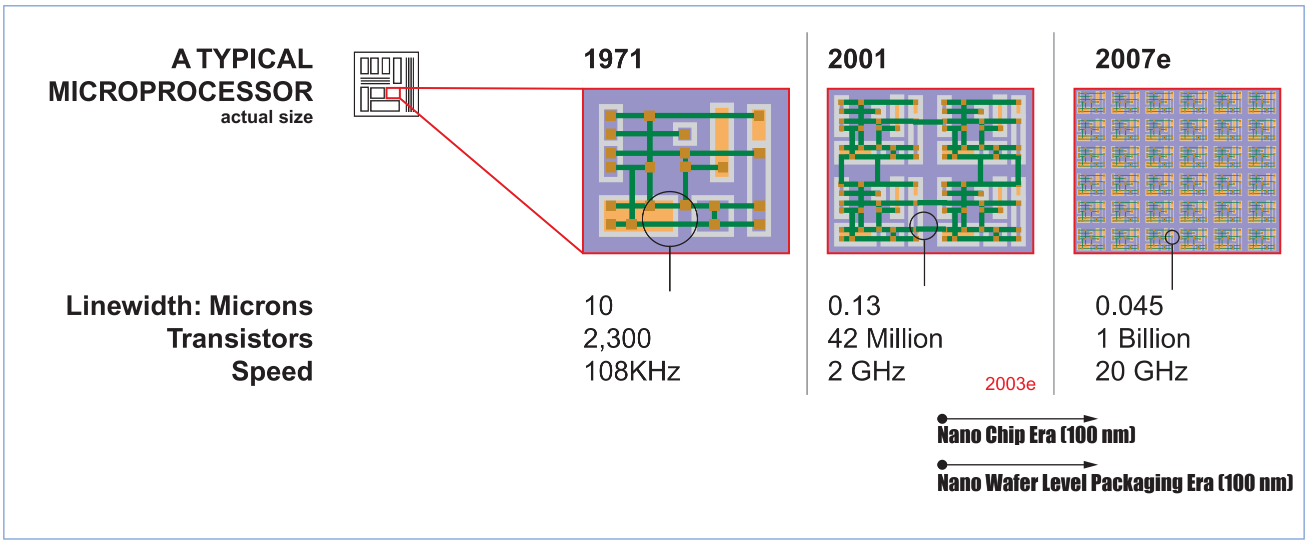
Journey to Nano Wafer Level Packaging

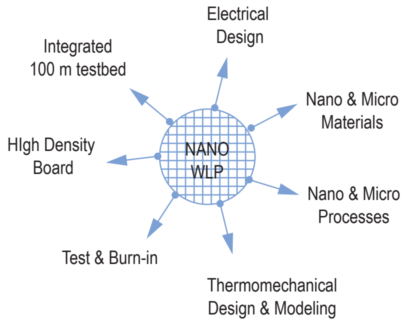
Nano Chips Require Nano Packaging: Information Technology (IT) is more than a trillion dollar industry. It includes hardware, software, services and applications. Contrary to the perception, the hardware accounts for better than two thirds and the single most important building block of this hardware, of course, is semiconductor devices such as CMOS, Ga -As, Si- Ge, Silicon- on-insulator for a variety of digital, RF, analog and optoelectronic applications. The total worldwide annual market for these devices is about $150- 200 B. These devices, the technology for which is at the threshold of Nano scale (100nm), are typically fabricated into wafers as big as 300 mm in diameter and are subsequently diced into individual ICs. They are then packaged, tested, and burned into individual IC devices ready to be surface mount bonded onto system level boards. The total number of ICs produced in year 2000 was about 375B units, each packaged at some cost, typically $0.01U.S. per I/O. The total packaging market, which includes IC Packaging as well as systems packaging, is almost as big as the semiconductor market, together accounting for 25% of IT.

Our Vision: The semiconductor industry is racing toward a historic transition- Nano chips with less than 100 nm features. The first set of chips should reach production in 2003. Some of these chips will have several hundred million transistors, which require I/Os in excess of 10,000, power in excess of 200 Watts, providing computing speed in terabits per second.

How Are They Going to be Packaged? They require Nano packaging. Nano packaging comes at two levels: wafer level and system board level. This Temasek Professorship focuses on wafer level.

What is a Wafer Level Package and Why? A wafer-level package is one in which the die and "package" are fabricated and tested on the wafer prior to singulation. Nano wafer level packaging uses Nano materials and structures to bring about unprecedented advances in electrical, mechanical, and thermal properties in the chip-to-package interconnections.



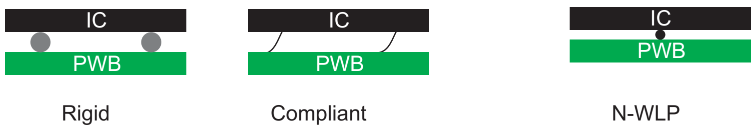


Seven Areas of Cross-disciplinary Leading-edge Research

The Benefits of Wafer Level Packaging are Several:

1. Smallest IC package size as it is a truly chip-size package (CSP);
2. Lowest cost per I/O because the interconnections are all done at the wafer level in one set of parallel steps;
3. Lowest cost of electrical testing as this is done at the wafer level;
4. Lowest burn-in cost as burn-in is done at the wafer level;
5. Potentially eliminates underfilling with organic materials around the solder joint;
6. Enhances electrical performance because of the short interconnections.

Current **Proposed**

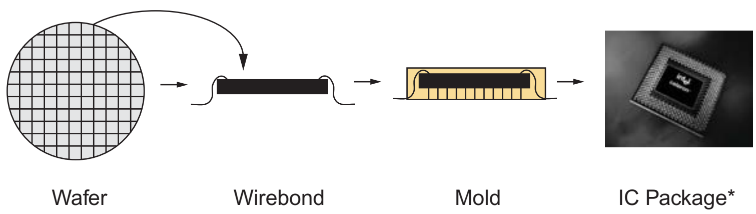


	Current	Proposed
Pitch	225-300 microns	20-100 microns
Speed	2 GHz	20-50 GHz
Power	75 Watts	200+ Watts
Cost/IO	$.01 USD	10X Lower

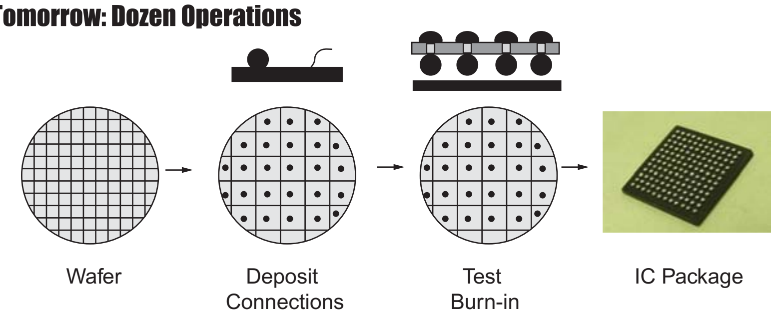
Proposed Research: The objectives of the proposed research are to lower cost and improve I/O pitch by an order of magnitude and yet support 20-50 GHz digital and RF applications, some of which require power in excess of 200 watts.

The barriers to achieving these objectives are many.   They will be overcome by seven focus areas of research:
1. Electrical design;
2. Nano and Micro materials;
3. Nano and Micro interconnection processes;
4. High density board
5. Thermo-mechanical design, modeling and analysis;
6. Test and burn-in at wafer level;
7. Integrated testbed that demonstrates a 100 micron pitch wafer level packaging system.

Today: Million Operations for 1000 Chips each at 1000 I/Os



Tomorrow: Dozen Operations



**IC photo courtesy of Intel*

Electrical Design

Objectives: Maintaining signal integrity represents one of the major bottlenecks for enabling reliable systems. This is due to the increase in speed, reduction in voltage, increase in power, and the integration of mixed signal functions in future systems. Examples of such systems include electro-optic USB interfaces, wireless devices, server farms and computing applications. Due to the fast transition of digital signals, the analog behavior of these signals becomes very important. Issues such as cross talk, reflections, switching noise, eye patterns and delay, therefore, have to be addressed for the design of systems. Wafer level packaging of circuits provides a very attractive solution for future micro-systems, especially in the mobile computing area. This is because of reduced parasitics and smaller form factor.

Approach: The combination of wafer level packaging and a high-density printed circuit board with embedded functionality has many advantages for the design of mixed signal Nano systems. The wafer level package reduces parasitics through short compliant or rigid leads, improves isolation by separating incompatible circuitry and enables much better matching of components for developing integrated solutions. Both modeling and experimental techniques will be pursued. In particular, the following electrical issues will be studied in detail: 1) design of the chip-to-package compliant or rigid leads and transitions for supporting digital and RF signals 20-50GHz; 2) design of the chip-to-package compliant and rigid leads to supply >200W of power to the chips with minimum power supply noise and electro-migration problems and; 3) study of transmission line and radiation effects of the chip-to-package compliant or rigid leads for supporting 20-50GHz digital signals.

Research Focus:

- Design of the transitions from the chip into the high-density printed circuit board through the compliant or rigid leads. Modeling tools and measurement techniques will be used for the design of these transitions.

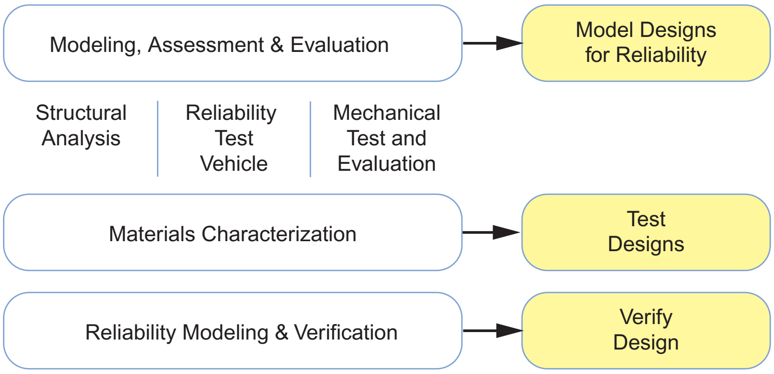
- Design of the compliant or rigid leads with minimum inductance that can support fast transient currents for supporting multi-gigahertz digital circuits dissipating > 200W of power. Power distribution analysis tools developed at Georgia Tech will be enhanced to model the geometries. These will be correlated with measurements on custom chips.

- Modeling of the current density through the compliant or rigid leads to estimate high frequency current densities and their effect on electro-migration.

- Radiation and transmission line measurements to better understand the electromagnetic behavior of the leads at frequencies 20-50GHz.

Design, Modeling and Reliability

Objectives: With the continued reduction in IC feature size and with the increased demand for better performance and lower cost, there is a need for an innovative, yet reliable, interconnect technology. According to the NTRS roadmap in the U.S., the interconnect pitch, will be less than 50 microns, and in select opto-electronic applications, it can be as small as 10 microns. Most of the existing interconnect technologies today, even with dramatic improvements, are incapable of addressing this ultra-fine pitch requirement. Therefore, there is a compelling need to understand the thermo-mechanical design requirements, failure mechanisms and reliability of such interconnects and develop suitable interconnects starting with design for reliability.



General Interconnection Design and Optimization Scheme

Approach: To cater to the CTE mismatch between the die and the substrate, two basic designs of ultra-fine pitch interconnections have been proposed: compliant and rigid. A compliant interconnection reduces the stress but tends to yield lower electrical performance and mechanical flimsiness compared to rigid interconnections. On the other hand, rigid interconnections have to sustain higher stresses resulting in likely failures by fracture or fatigue. However, this deficiency may be overcome by the use of high-strength Nano-structured materials. The mechanical, thermal and electrical characteristics of various interconnection designs falling under the two main categories will be studied extensively through modeling and simulation and a few likely-to-succeed designs will be identified. Specimens of the short-listed designs will then be fabricated and the material properties and processes characterized. Constitutive models of new materials will be obtained. The state of stress in the interconnections will be modeled for the entire fabrication process in order to predict more precisely the reliability of the final product. Extensive reliability tests will also be conducted in order to study the failure mechanisms operating. Models of these failure mechanisms will be developed and used to predict the reliability of the final product. With such models developed, the design of the interconnections can be further optimized through simulation and experimental verification.

Research Focus:

- Design:
  - Propose potential solutions for 100 micron and 20 micron pitches;
  - Critical evaluation of characteristics and challenges of each solution.

- Modeling:
  - Develop methodology for modeling material properties and processes;
  - Develop comprehensive models to predict failure mechanisms operating;
  - Develop integrated modeling methodology and design for reliability of WLP;
  - Explore the use of molecular dynamics and multi-scale modeling in reliability prediction of WLP.

- Materials Characterization:
  - Conduct experiments to characterize the properties of materials including Nano-structured materials;
  - Develop constitutive models of relevant materials.

- Failure Analysis and Reliability Tests:
  - Design and conduct reliability tests to study the operative failure mechanisms;
  - Develop failure analysis techniques and methodology to characterize the failure mechanisms;
  - Demonstrate reliability of testbed.

Wafer Level Interconnect Approaches

Objectives: The overall objective is to develop fine pitch and low cost interconnect technologies for high-density wafer level packaging. The current wafer level packages are at a pitch of 300-400 microns, serving primarily memory products. The proposed pitch will explore different wafer level interconnect technologies for 20 micron and demonstrate 100 micron pitch meeting the electrical, thermal and mechanical requirements.

Approach: With the need of 20 to 100 micron pitch, both rigid and compliant interconnect structures will be pursued in this thrust area. A total of 6 different wafer level interconnect schemes are proposed:

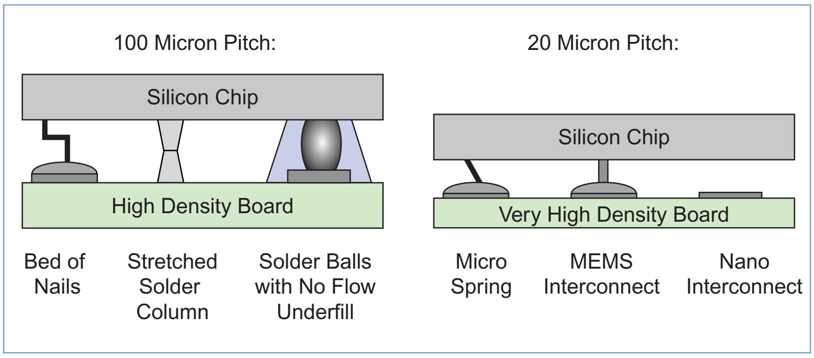
a) 100 micron pitch
- Bed of nails (compliant)
- Streched solder column (rigid)
- Lead-free solder balls with no flow underfill (rigid)

b) 20 micron pitch
- Nanostructured interconnect based on polymer-metal or metal-metal interfacial composites (rigid)
- Nano springs (compliant)
- MEMs-fabricated interconnects (compliant)

The wafer level packages with 100 micron pitch will be assembled into the final integrated test bed. The wafer level packages with 20 micron pitch incorporates Nano interconnects and will be studied form a research point of view.

Research Focus:

- Explore and demonstrate promising materials and processes for 20 micron and 100 micron pitch wafer level interconnect schemes;
- Select or develop metal and lead-free solder alloys and develop new characterization methodologies;
- Develop the processes involved in fabricating the interconnections;
- Optimize various processes for 100 micron scheme.



Wafer Level Interconnect Scheme

Potential of Nano-Structured Materials

Objectives: The most aggressive wafer level packaging proposed is on 20 micron pitch. At this pitch, the conventional solder ball technology does not guarantee the reliability of the IC-to-board joint. Compliant connection is one solution but it may be expensive and it may not provide the best electrical properties. Underfill around the solder is another solution but it makes the process complex and makes the technology expensive too. Nano interconnection is proposed because of its potential unique mechanical and electrical properties.

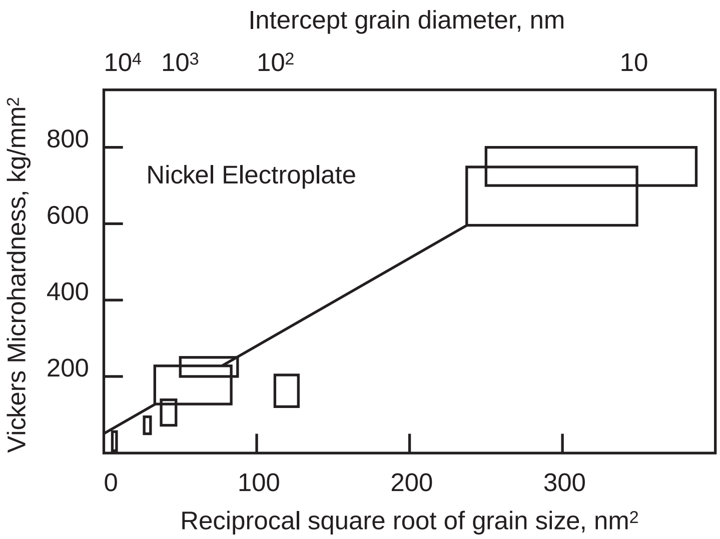
Approach: Experimental studies have demonstrated that there is considerable potential for enhancing strength of materials through interface strengthening (increasing grain boundary area and/or phase boundary area) in several material systems such as Cu, Ni, Ni-base alloys and intermetallics, aluminum alloys, gold, and carbon steels. Mechanical strengthening in crystalline materials occurs as a result of obstacles encountered by dislocations restricting their mobility. Obstacles to dislocation motion are in the form of (a) lack of appropriate number of primary slip systems (b) coherent and incoherent precipitates (c) interphase and antiphase boundaries and (d) grain boundaries. Thus, reducing microstructural features to the Nanometer scale and creating more such obstacles in the process, provides avenues for tailoring strength, toughness, and creep properties, in addition to influencing electrical resistivity and solid-state diffusivity and solubility.

Research Focus:

- Identify promising Nano-stuctured materials systems for use in 20 micron pitch interconnects and produce them in experimental quantities for evaluation. The range of materials to be considered include monolithic metals and alloys as well as composites containing Nano-structured metals and alloys as particulate reinforcements and conductive polymers as matrix;

- Characterize the materials to obtain tensile strength, hardness, fracture toughness and fatigue properties, and electrical properties, using novel techniques such as Nano indentation, in-situ AFM/STEM, SEM. Develop new characterization techniques as needed;

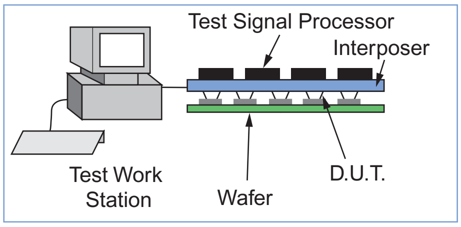
- Develop modeling and simulation tools to extract most information from tests and to aid in developing in-depth understanding of phenomena at the Nano level for its fullest exploitation in wafer level interconnect applications.

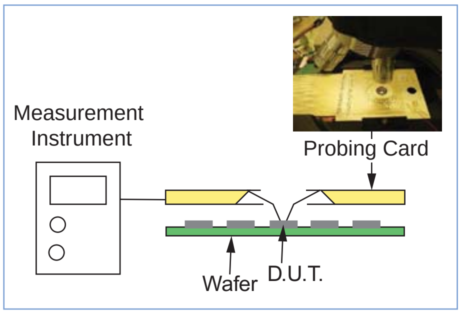


Microhardness of electroplated nickel as a function of reciprocal of the square root of grain size (Neiman, Weertman, and Siegel, 1991)

Test and Burn-In System

Objectives: Wafer level packaging is incomplete without guaranteeing Known Good Die (KGD). In conventional IC packaging it is done by test and burn in after the IC is packaged as QFP, BGA or CSP. But this individual test and burn-in at the IC level is a sequential and expensive process. The objective of this task is to develop strategies and implement them at 100 micron pitch at wafer level.





Approach: The need to make electrical contacts to the interconnecting structures with pitches of 20-100 microns presents tremendous challenges. Furthermore, the bandwidth requirements present tremendous challenges to the selection of materials as well as integration and fabrication methods. Presently, testing of wafer-level packaged devices is performed using fine-pitch probes directly on the wafer. It is expected that this approach will not be applicable to the Nano wafer level.

An interposer, with a self-aligned, z-axis compliant and good electrical contact features, will be designed and fabricated to serve as the electrical and mechanical interface between the N-WLP and the tester. Due to the large number of inputs/outputs on this N-WLP (in the order of 10,000 to 200,000 I/Os per cm^2, it is anticipated that this interposer will not be able to handle the required re-distribution task. As such, a test support processor (TSP) board consisting of a field-programmable array device, memory devices, sample-and-hold devices, clocks, multiplexers, and others, will be integrated onto the top layer of the interposer, using the flip chip attachment method. The test signal processor will act as the tester with the required test stimuli and memory to capture the tested data. In this way, only a few I/Os from the TSP are required for each wafer level-packaged device.

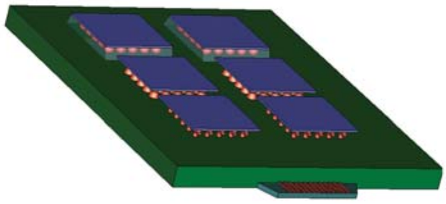
A burn-in system that simultaneously connects devices on several N-WLP ICs will also be developed. As in most burn-in requirements, the task of re-distributing the vast number of I/Os may not be the limiting factor as only specific electrical connections are required during burn-in. An interposer, similar to the interposer developed for wafer-level test, will be developed to serve as the electrical and mechanical interface for burn-in.

Research Focus: Besides fabrication challenges, the other major challenges will be the selection of materials and integration methods to meet the large bandwidth requirements of the interposer.

- Design and fabrication of the interposer
- Design and fabrication of the test signal processor
- Integration of the test signal processor onto the interposer to form the TSP interposer
- Test and characterization of the TSP interposer
- Design and fabrication of a burn-in interposer
- Integration of the burn-in interposer into a burn-in system
- Optimization of test and burn-in strategy for NWLP

Integrated Wafer Level Test Bed

Objectives: The objective is to design and assemble an integrated test bed to demonstrate 100 micron pitch reliable wafer level packaged system. The test bed shall integrate all the above wafer level packaging technologies including the test and burn-in to mee the required mechanical and electrical integrity.



Approach: The approach would be to integrate all the enabling technologies into a testbed. The proposed specification for 100 micron pitch wafer level packages will be designed into the testbed. The challenges from electrical signal integrity and thermo-mechanical reliability would be addressed in the 100 micron pitch testbed design and development. The testbed is also intended to demonstrate the wafer level packaging materials and processes. The electrical testing will be done in two phases: 1) DC testing, demonstrating the technologies; and 2) functional testing, demonstrating the test features and compatibility of the technology to testing.

Proposed Target Specification of the Nano Wafer Level Packages

Specification:	State of the Art Today:	Proposed: 100 Micron	Proposed: 20 MIcron
Acceptable Cost	U.S. $50 to $150	0.5X	0.1X
Electrical	Digital and RF 2-3 GHz	Digital and RF 10 GHz	Digital and RF 20-50 GHz
Thermomechanical Reliability	JEDEC Level 3	JEDEC Level 2 Board Level Reliability	
Die Size	7mm (0.8 sq. cm)	20 mm (4 sq. cm)	20 mm (4 sq. cm)
Pitch	50 µm	100 µm	20 µm
Distance from Neutral Point	<5 mm	10-14 mm	10-14 mm
I/O per cm^2	340	8100	>10,000
Interconnect Size	300 µm	30 µm	6-8 µm
Applications	Memories, Passives, RF-Ids	Handheld Computing	High Performance Computing
Manufacturability	Batch Processing	Batch Processing	Batch Processing
Enbabling Technology	RDL, UBM	Comliant, Rigid Test and Burn-in	Nano Interconnect Materials Characterization, Processes,Test and Burn-in

Research Focus:

- Develop electrical design and simulation methodologies of the test bed to accommodate 100 micron pitch wafer level packages. The design and characterization techniques used at the wafer level interconnects would be extended to the system test bed keeping in mind the 20-50GHz bandwidth goal;
- Exploration and assessment of the thermo-mechanical reliability.
- DC level testing and burn-in integrated into the board. The test strategies developed at the wafer level would be extended to board level testing;
- Design and development of 100 micron board demonstrating the compatibility between the 100 micron pitch wafer and the 100 micron board.

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